

Intel Developer Forum.



**designing
platform
solutions**

intel®

Intel Developer Forum

Albert Yu
Senior Vice President
Microprocessor Products Group
Intel Corporation

September 15, 1998

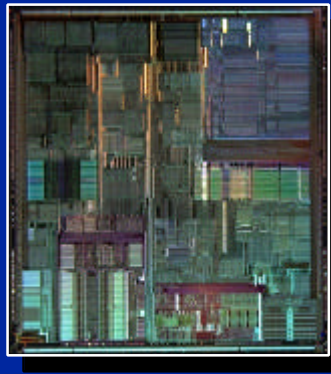
Agenda

- **New Technologies**
- **Compelling Products for Every Segment**
- **Summary**

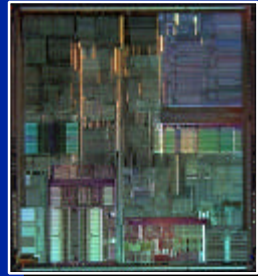
Agenda

- **New Technologies**
 - Silicon Technology
 - Validation Technology
 - Katmai New Instructions
- **Compelling Products for Every Segment**
- **Summary**

Technology Trends



.6μ



.35μ



.25μ



.18μ



.13μ



.1μ

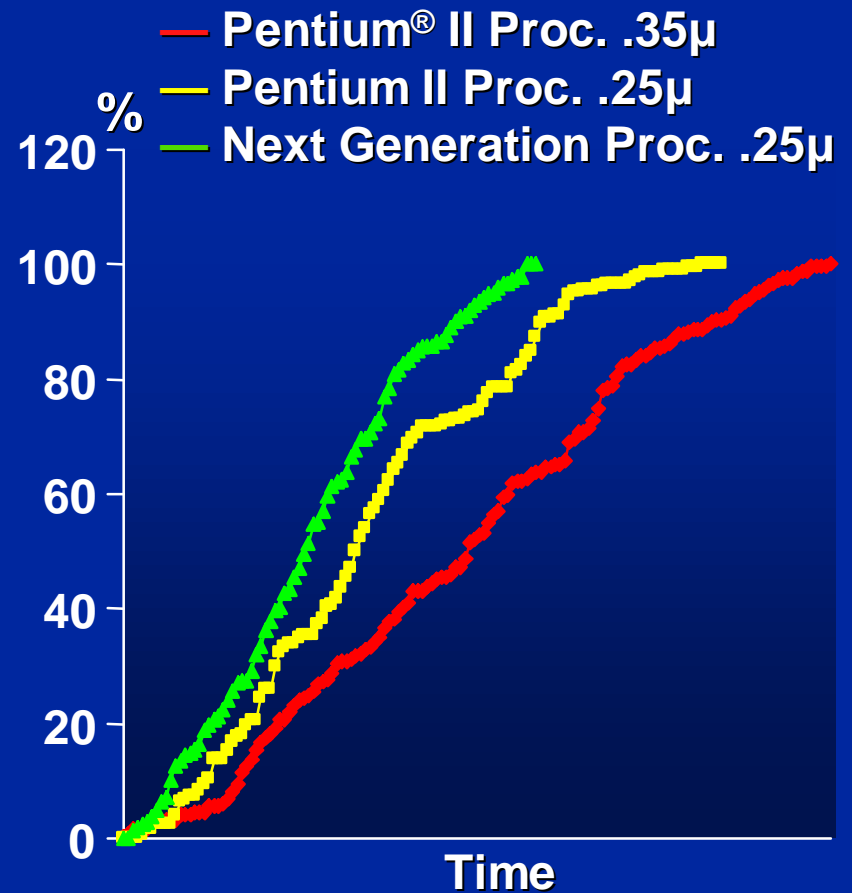
Line Width Shrinks

Agenda

- **New Technologies**
 - Silicon Technology
 - Validation Technology
 - Katmai New Instructions
- **Compelling Products for Every Segment**
- **Summary**

Validation Technology

- Design for correctness
 - Formal verification
 - Cluster level validation
 - System level co-simulation
- The big test
 - Thorough 24X7 testing
 - Coverage based testing
 - Segment specific stresses (servers, desktop, mobile...)



Validation Technology



- **Stress testing:**
 - 124 Intel servers & 1072 clients
 - >50K stress hours
 - >30 Miles of Cat5 Network, multiple protocols
 - >30 stress workloads, >30 system configurations
 - Win NT*, Win '9X*, Win 3.x, OS/2*, SCO*, Unix*, Netware*, Unixware*
 - 75×10^{18} cycles

Agenda

- **New Technologies**
 - Silicon Technology
 - Validation Technology
 - **Katmai New Instructions**
- **Compelling Products for Every Segment**
- **Summary**

Katmai New Instructions

- **New architecture enhancements**
 - Increase performance
 - Reduce system bottlenecks
- **Improved handling of rich data types**
 - Real-time MPEG2 encode/decode
 - Faster, richer 3D graphics
 - AC3 audio
 - Continuous, accurate speech recognition
 - Complex imaging effects
 - Realistic movement physics

Katmai New Instructions

Dynamic Execution

Multi-Transaction
P6 Bus

MMX™ Technology

Current P6
Microarchitecture

Katmai New Instructions

Dynamic Execution

Multi-Transaction
P6 Bus

MMX™ Technology



Memory Streaming
Architecture

New Media
Instructions

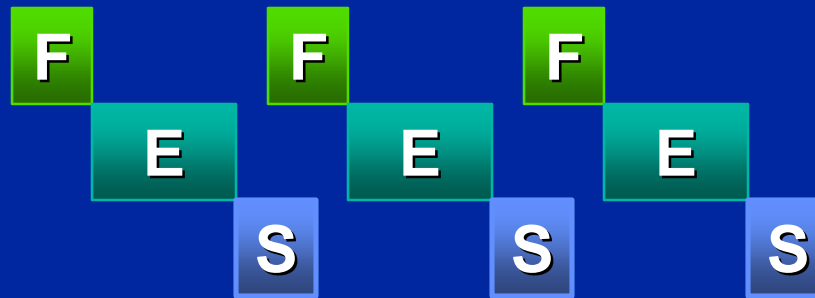
Concurrent SIMD-FP
Architecture

Current P6
Microarchitecture

Katmai New Instructions

Memory Streaming Benefits

*Without
Memory
Streaming*



*With
Memory
Streaming*



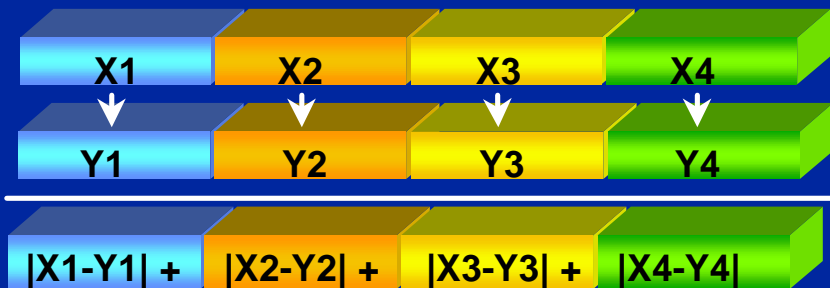
Time —————>

***Streaming Hides Memory Latency
Under Software Control***

New Media Instructions

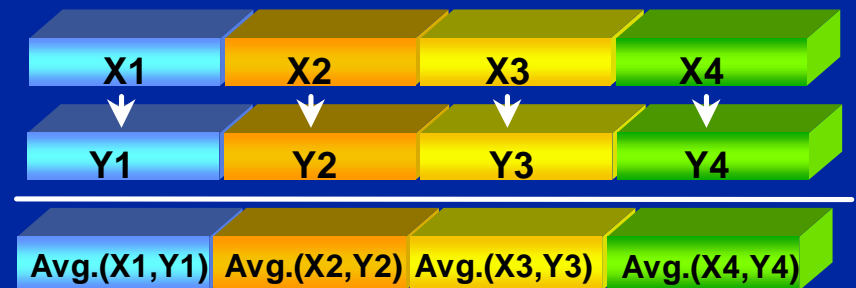
Sum of Absolute Differences

Video encode: motion estimation



Average w/Rounding down

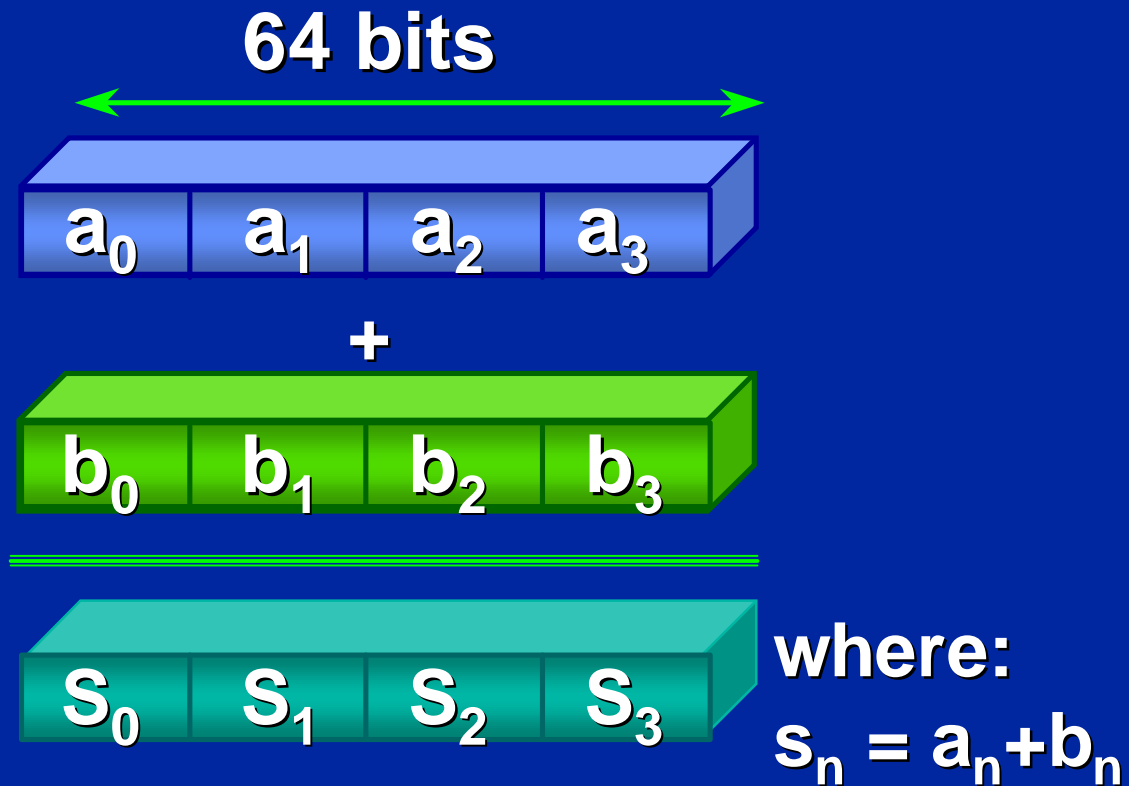
Video decode: motion compensation



Additional New Media Instructions

- Packed Maximum
 - Packed Minimum
- Speech Recognition

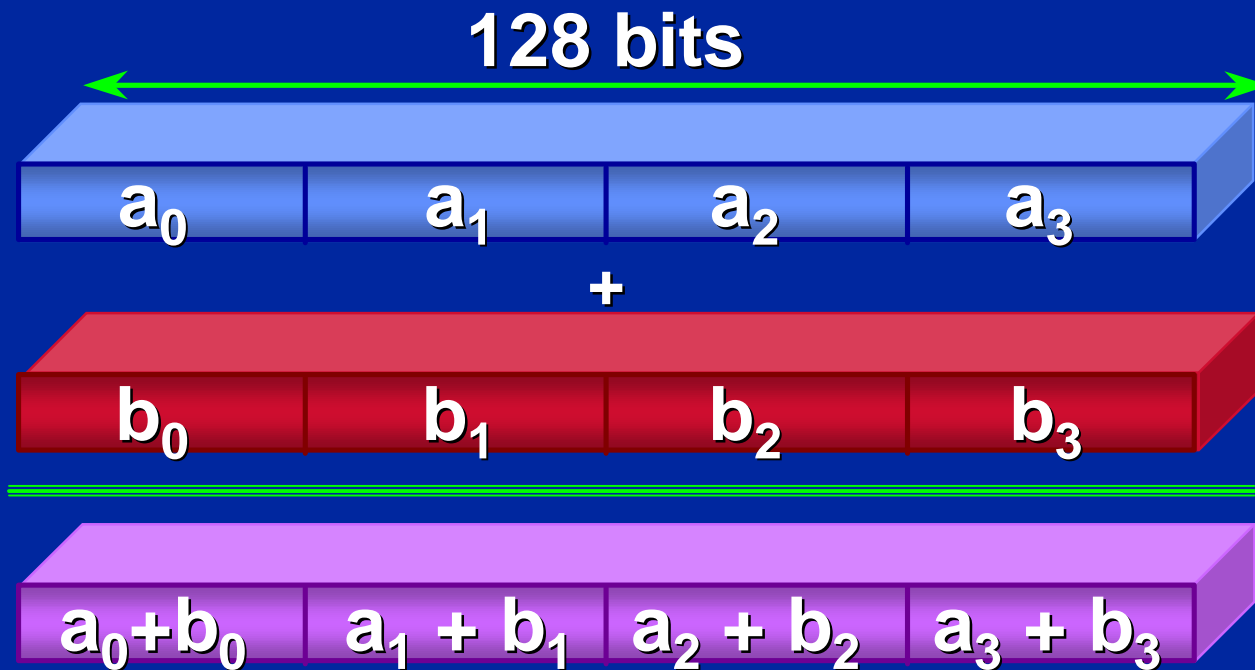
MMX™ Technology



Packed Integer Op./Instruction

Katmai New Instructions

SIMD Architecture for FP Data



4-wide Single Precision Packed
Single Op./Instruction

intel® **500MHz Katmai/Tanner = 2 GFlops/sec Peak**

Agenda

- New Technologies
- **Compelling Products for Every Segment**
- Summary

Server/Workstation



Pentium® II Xeon™ Processors

Launch

1998

Processor

Pentium II Xeon

L2 Cache

512K, 1M, (2M)

Frequency

400/450 MHz

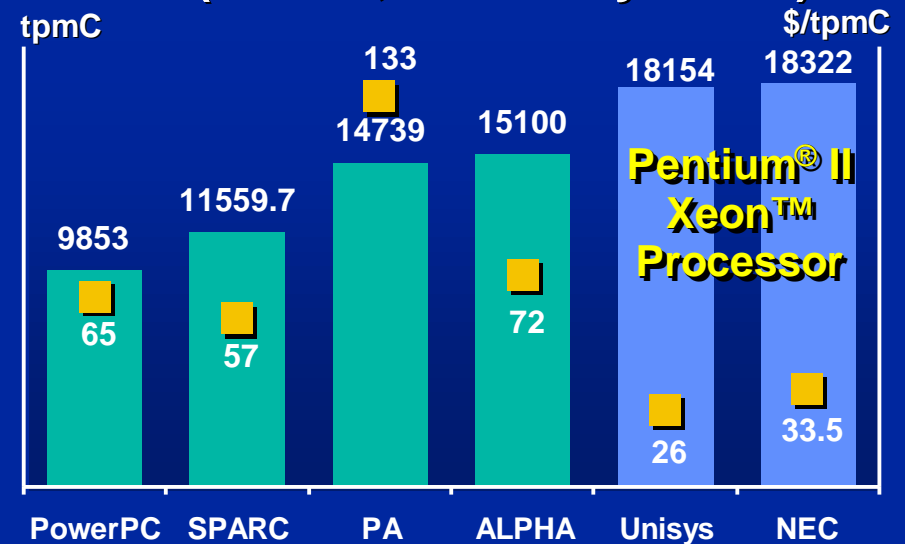
Package

S.E.C.C.

Chipset/Bus

450NX/100
440GX/100

Performance and Value: OLTP (TPC-C, 4 CPU Systems)



Source for Sun, HP, IBM and Compaq results: TPC Website (www.tpc.org). Pentium II Xeon processor performance measurements audited and submitted by Unisys and Compaq to TPC 6/29/98. TPC-C is a benchmark from the Transaction Processing Council (TPC Benchmark™ C).

Server/Workstation



Pentium® II Xeon™ Processors



Tanner Processors

Launch

1998

1H'99

Processor

Pentium II Xeon

Tanner (0.25μ)

L2 Cache

512K, 1M, (2M)

512K, 1M, 2M

Frequency

400/450 MHz

500 MHz

Package

S.E.C.C.

S.E.C.C.

Chipset/Bus

450NX/100
440GX/100

450NX/100
440GX/100

Server/Workstation



Pentium® II Xeon™ Processors



Cascades Processors

Launch

1998

2H'99

Processor

Pentium II Xeon

Cascades (0.18μ)

L2 Cache

512K, 1M, (2M)

TBD

Frequency

400/450 MHz

>500 MHz

Package

S.E.C.C.

S.E.C.C.

Chipset/Bus

450NX/100
440GX/100

TBD

Performance PC



Pentium® II Processors

Launch

1998

Processor

Pentium II

L2 Cache

512K BSRAM

Frequency

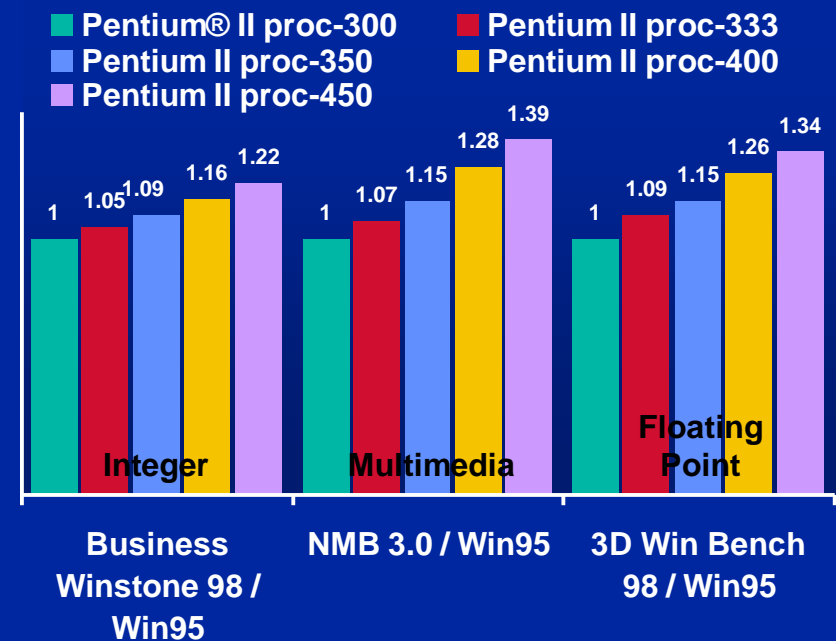
350,400,450 MHz

Package

S.E.C.C.

Chipset/Bus

440BX/100



Source: Intel MAP. Performance PC Configuration: Intel SE440BX Motherboard; 32MB SDRAM, Seagate SCSI disk, Matrox Millennium II/AGP, 3D Win Bench measured on STB Velocity 128/AGP; Microsoft DirectX 5; L2 ECC Disabled.

Performance PC



	Pentium® II Processors	Katmai Processors
Launch	1998	1H'99
Processor	Pentium II	Katmai (0.25μ)
L2 Cache	512K BSRAM	512K BSRAM
Frequency	350,400,450 MHz	450 & 500 MHz
Package	S.E.C.C.	S.E.C.C. & S.E.C.C.2
Chipset/Bus	440BX/100	440BX/100

Performance PC



	Pentium® II Processors	Coppermine Processors
Launch	1998	2H'99
Processor	Pentium II	Coppermine (0.18μ)
L2 Cache	512K BSRAM	TBD
Frequency	350,400,450 MHz	>500 MHz
Package	S.E.C.C.	S.E.C.C.2
Chipset/Bus	440BX/100	TBD

Basic PC



Celeron™ Processors

Launch

1998

Processor

Celeron™

L2 Cache

128K Integrated

Frequency

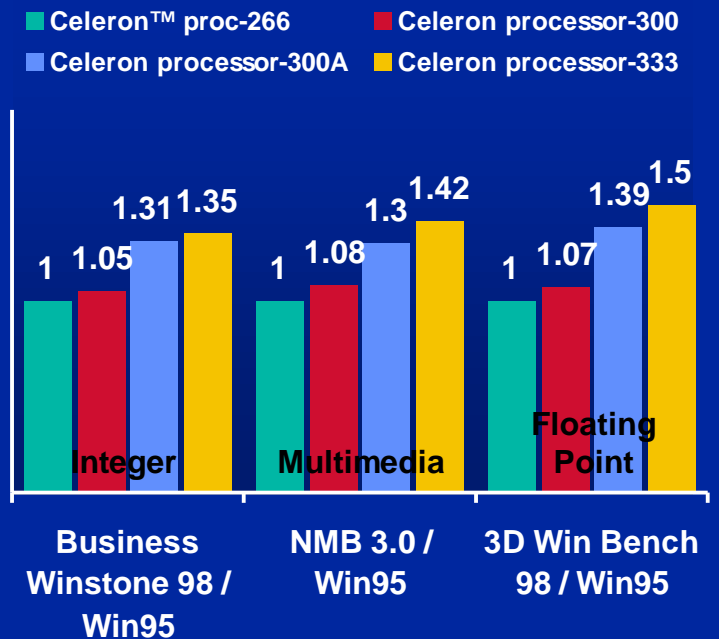
300A, 333 MHz

Package

SEPP

Chipset/Bus

440LX/EX



Source: Intel MAP. Basic PC Configuration: Celeron on 440EX, PP/MT on 430TX; 32MB SDRAM, Seagate EIDE disk, ATI 3D Rage Pro; 3D Winbench measured on STB Velocity 128; Microsoft DirectX 5.

Basic PC



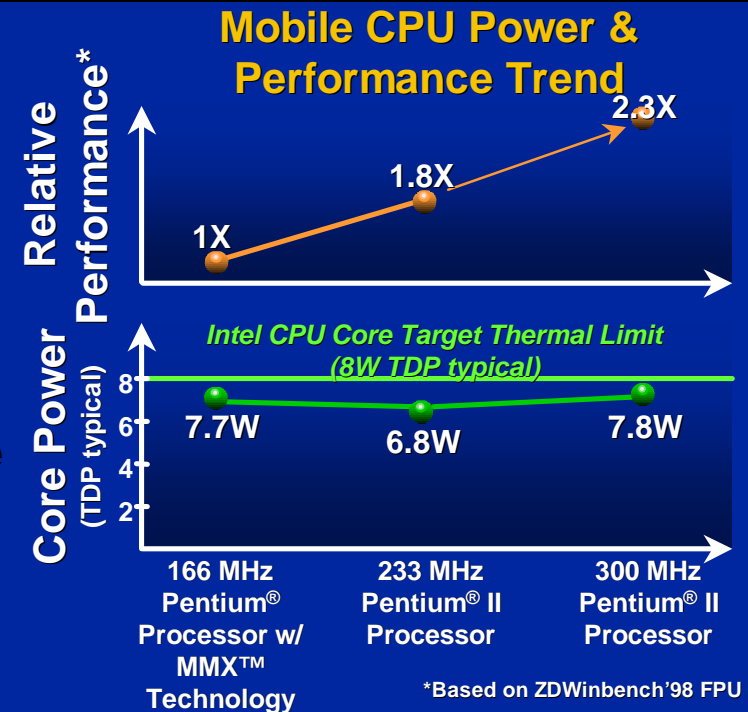
	Celeron™ Processors	→	Celeron™ Processors
Launch	1998		1H'99
Processor	Celeron™		Celeron™
L2 Cache	128K Integrated		128K Integrated
Frequency	300A,333 MHz		366 MHz
Package	SEPP		SEPP/PPGA
Chipset/Bus	440LX/EX		440LX/EX

Mobile PC



Mobile Pentium® II Processors

Launch	1998
Processor	Mobile Pentium II
L2 Cache	512K PBSRAM
Frequency	233,266,300 MHz
Package	Mini-Cartridge Module
Chipset/Bus	440BX/66



Mobile Pentium® processor with MMX™ technology at 166/200/233/266 MHz ran on Gateway® Solo 9100 system with Intel 430TX/PCiSet-based mobile module, 512K L2 cache, 32MB SDRAM, 2.1GB HDD, 8X-20Xmax CD-ROM, C&T 65554 graphics controller; Mobile Pentium® II processor 300/266/233 MHz ran on Gateway® Solo 2500 w/ Intel 440BX mobile module, 512K L2 cache, 32MB SDRAM, 2.1GB HDD, 8X-20Xmax CD-ROM, MagicGraph® 128XD graphics controller.

Mobile PC



	Mobile Pentium® II Processors	Mobile Pentium® II Processors
Launch	1998	1H'99
Processor	Mobile Pentium II	Mobile Pentium II
L2 Cache	512K PBSRAM	TBD
Frequency	233,266,300 MHz	>333 MHz
Package	Mini-Cartridge Module	Mini-Cartridge Module
Chipset/Bus	440BX/66	440BX/66

Segmented Product Roadmap

'98

'99

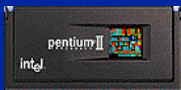


**Server/
Workstation**

**Pentium® II Xeon
Processors**



**Tanner and
Cascades
Processors**



**Performance
PC**

**Pentium® II
Processors**



**Katmai and
Coppermine
Processors**



Basic PC

**Celeron™
Processors**



**Celeron™
Processors**



Mobile PC

**Mobile Pentium® II
Processors**



**Mobile
Pentium® II
Processors**



**Set Top Box
Handheld**

**StrongARM*
Processors**



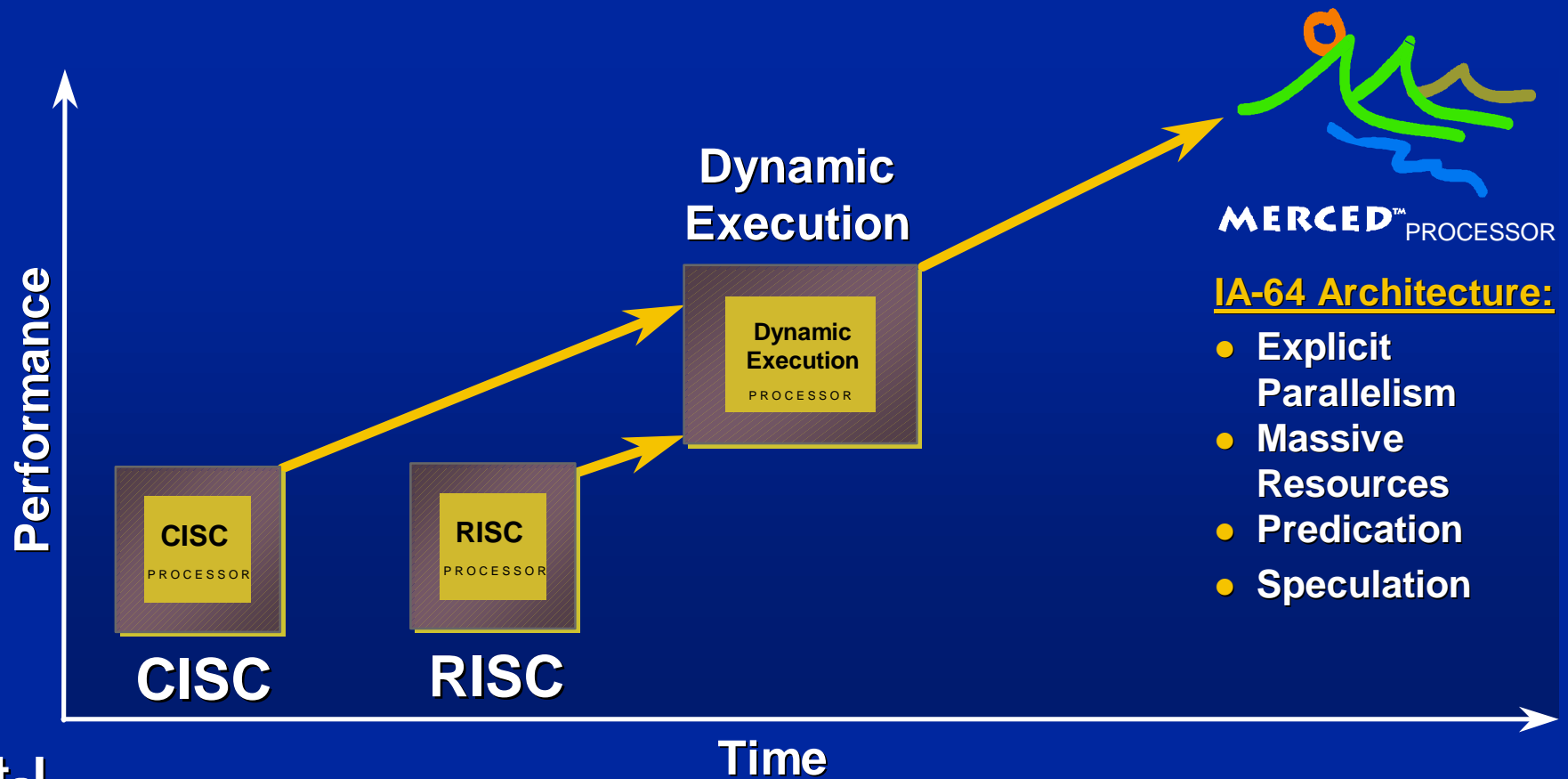
**StrongARM*
Processors**

intel®

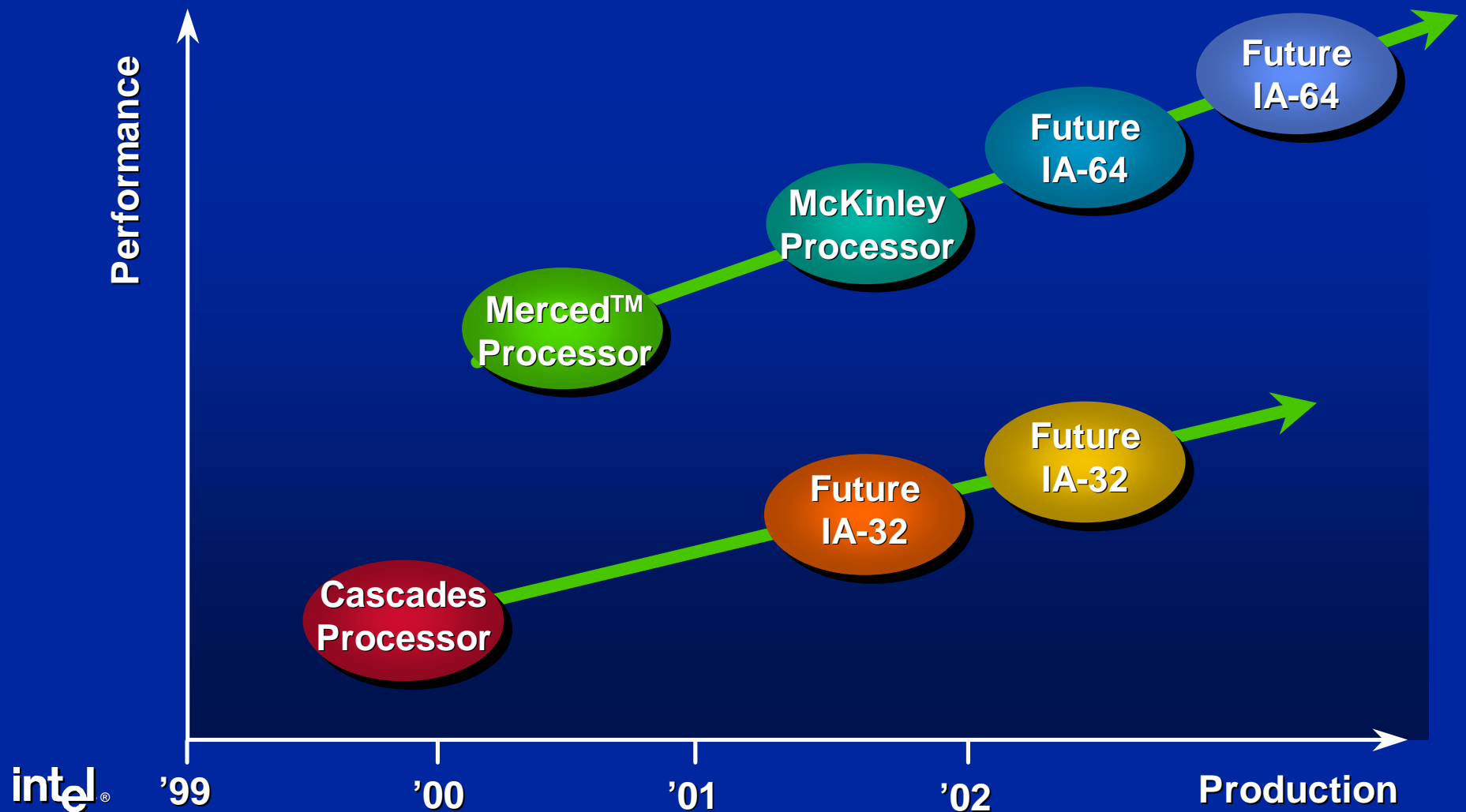
*Other brands and names are the property of their respective owners.

IA-64 Architecture: EPIC Technology

Explicitly Parallel Instruction Computing



Server/Workstation Processor Roadmap



Summary

- Intel provides leading edge Technologies
 - Silicon Technology
 - Validation Technology
 - Katmai New Instructions
- Intel's roadmap has never looked stronger
- Build your successful business with our compelling products

Intel Developer Forum.



**designing
platform
solutions**

intel®